

Design of capacitor-less LDO regulator with high reliability ESD Protection circuit using analog switch structure for 5 V applications

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Abstract

This letter suggests to the LDO regulator with the high reliability ESD protection circuit that achieves low peak voltage through analog switch structure. The proposed LDO regulator has the function of detecting the output voltage fluctuations depending on the load via an analog switch structure and effectively controlling the peak voltage. The proposed ESD protection circuit is placed on I / O and power lines to prevent the IC circuit from being destroyed from the inevitable ESD phenomenon. It was verified that the reliability of the IC can be improved through effective current discharge due to ESD surge. The proposed LDO regulator, implemented in a 0.18 μ m BCD process, achieves an undershoot voltage of 25 mV and an overshoot voltage of 28 mV for a load current of 300 mA.

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