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February 3, 2023

# SEVDA: Singular Value Decomposition Based Parallel Write Scheme for Memristive CNN Accelerators

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***Abstract*—Von Neumann architecture-based deep neural network architectures are fundamentally bottlenecked by the need to transfer data from memory to compute units. Memristor crossbar-based accelerators overcome this by leveraging Kirchoff's law to perform matrix-vector multiplication (MVM) in-memory. They still, however, are relatively inefficient in their device programming schemes, requiring individual devices to be written sequentially or row-by-row. Parallel writing schemes have recently emerged, which program entire crossbars simultaneously through the outer product of bit-line and word-line voltages and pulse widths respectively. We propose a scheme that leverages singular value decomposition and low-rank approximation to generate all word-line and bit-line vectors needed to program a convolutional neural network (CNN) onto a memristive crossbar-based accelerator. Our scheme reduces programming latency by $90\%$ from row-by-row programming schemes, while maintaining high test accuracy on state of the art image classification models.**

***Index Terms*—Convolutional neural networks, hardware accelerator, in-memory computing, Singular Value Decomposition, resistive RAM.**

## I. INTRODUCTION

Machine learning algorithms have experienced rapid advances in recent years, largely fueled by the ever increasing scale of machine learning models and datasets [1]. Deep neaural networks (DNNs) in particular, which are neural networks with many layers and interconnections between layers, have seen enormous success in their application to fields such as computer vision with the use of convolutional neural networks (CNNs) [2], and natural language processing through the use of recurrent neural networks (RNNs) [3]. This increased scale has been accompanied by an increased need for computational resources, prompting many different hardware acceleration platform designs to fulfil this need [4-6]. These architectures still suffer from the off-chip memory bottleneck inherent to the Von-Neuman computer architecture [7], however. Memristor crossbar based accelerators solve this by performing in-memory matrix vector multiplication [8-9]. It remains a challenge, however, to program crossbar cells to the desired weight. Parallel writing schemes intended to decrease crossbar programming latency and energy consumption have been explored before [10-11], but none so far have explored how one may be implemented in a practical application, such as programming a CNN onto a memristor crossbar, as this would require a scheme which converts the weight data structures of the model into a set of word-line and bit-line voltages and pulse-widths. We achieve this by leveraging Singular Value Decomposition (SVD) and generating a low rank approximation of the model layers while minimising accuracy loss and delay.

## II. PRELIMINARIES

### A. Convolutional Neural Networks

Convolutional Neural Networks (CNNs) are a particular class of feed-forward deep neural networks, typically used for computer vision tasks [12]. In inference, these networks typically feature three types of layers: Convolutional layers (CONV), Fully Connected layers (FC) and pooling layers. CONV layers work by performing convolutions using learned parameters while scanning an input, the resultant output is commonly referred to as a feature map, as it extracts relevant features form its input. FC layers are usually found near the output of a network, as they are typically used to optimise class matching in multi-class classification networks. Their input is usually flattened and connected to all neurons in the layer. Pooling layers are typically used after a CONV layer, and they work by downsampling the input to reduce computational resource use. The most common types of Pooling layers are max and average pooling, which take the maximum and average of regions of the input map respectively.

### B. Crossbar based CNN Acceleration

In a crossbar architecture, each individual memristor device is connected to its corresponding word-line (WL) and bitline (BL) in a matrix layout similar to that of a conventional memory cell. MVM operations are achieved through the application of vector operands as analog voltages to the WL of the crossbar, as a result of Ohm's law, the current passing through the memristor cell is the product of the WL voltage and the device conductance G, and as a result of Kirchoff's current summation law, the BL current will be the sum of the currents passing through each cell in a given column. $I_j = \sum_{i=1}^{H} V_i G_{ij}$. Since device conductances cannot be negative, weights must be stored in a sign-magnitude form, where polarity is represented by two separate devices [13], as illustrated in figure 1b.

FC layers are the simplest operation to map onto the crossbar, as they can be represented as a simple matrix-vector

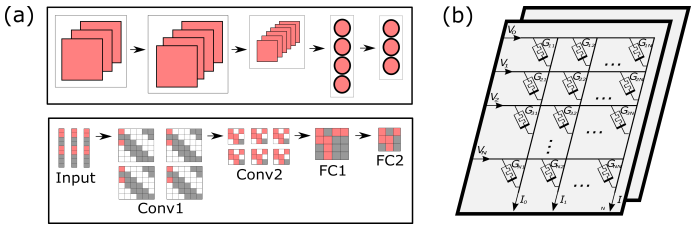


Fig. 1. (a) Illustration of the unrolling of a 5 layer CNN. (b) Crossbar structure.

multiplication, where the layer weights are the elements of a matrix $\mathbf{G}$ mapped to the device conductances, and the input activations are mapped to the WL voltage vector $\mathbf{V}$, such that the output activations are mapped to the BL currents. $\mathbf{I} = \mathbf{V}^\intercal\mathbf{G}$. Conv. layers require a more involved unrolling whereby convolutions are unrolled from

$$\begin{bmatrix} a_{11} & a_{12} & \dots \\ \vdots & \ddots & \\ a_{M1} & & a_{MN} \end{bmatrix} \circledast \begin{bmatrix} k_{11} & k_{12} \\ k_{21} & k_{22} \end{bmatrix} \tag{1}$$

to the following vector matrix multiplication [14].

$$\begin{bmatrix} a_{11} & a_{12} & a_{13} & \dots & a_{MN} \end{bmatrix} \times \begin{bmatrix} k_{11} & 0 & \dots & 0 \\ k_{12} & k_{11} & \dots & 0 \\ \vdots & \vdots & \ddots & \\ k_{21} & 0 & \dots & 0 \\ k_{22} & k_{21} & \dots & 0 \\ \vdots & \vdots & \ddots & \\ 0 & 0 & \dots & k_{22} \end{bmatrix} \tag{2}$$

Average pooling is mapped similarly to convolutions, with $k_{ij}$ always corresponding to $1/N^2$ where $N$ is the kernel size parameter. Max pooling, on the other hand, cannot be easily mapped to the MVM domain, and thus requires the use of dedicated CMOS hardware [15]. However, since max pooling is only typically found at the end of a chain of CONV and FC layers, and is generally not found in high proportion in most architectures, this should not present too great a bottleneck.

### C. Programming Conductance Values

Typically, crossbar cell conductances are programmed row-by-row, where the target row's WL and BL voltages are biased such that their product gives the desired conductance value. However, a quicker and more energy efficient way to program crossbars is through a parallel write, in which column inputs $x$ are encoded as voltage pulse-widths, while row inputs are encoded as voltage amplitudes $y$. The crossbar conductances $\mathbf{G}$ are thus updated according to the outer product of the row and column inputs. $\mathbf{G}_{i+1} = \mathbf{G}_i + x^\intercal y$. This technique creates the challenge of arriving at the correct row and column vectors to produce accurate weights, and how to schedule programming effectively.

## III. CNN Mapping Using Parallel Write

### A. SVD Based Parallel Write

In order to take full advantage of the parallel write capabilities of each memristor crossbar, we propose a technique which leverages Singular Value Decomposition (SVD) to decompose each matrix in use throughout the input CNN into a sum of outer products of vectors which may be applied as voltage amplitudes to the column inputs and as voltage pulse-widths to the column inputs of the crossbar tile. Since this is all done prior to deployment, we don not incur significant overhead, which is extremely beneficial for edge applications.

SVD is a technique which allows any matrix $\mathbf{A} \in \mathbb{C}^{mxn}$ to be expressed as $\mathbf{A} = \mathbf{U}\Sigma\mathbf{V}^*$ where $\mathbf{U}$ and $\mathbf{V}^*$ are square matrices of dimensions $m$ and $n$ respectively, and $\Sigma$ is an $m \times n$ diagonal matrix of singular values of $\mathbf{A}$ [16]. Since the singular value matrix is diagonal, the SVD can express a real conductance matrix of dimensions $m \times n$ as a sum of vector outer products, $\mathbf{A} = \sum_0^{minm,n} d_i p_i q_i^\intercal$. In order to preserve the efficiency of the parallel write scheme, we must take a low rank approximation of the conductance matrix $A$, as the number of outer products required to achieve an identical conductance matrix to the one desired is approximately equal to the input dimensions, as shown in figure 2b. To do this, we first employ a numeric rank regularization scheme intended to lower the effective rank of our fully connected matrices during fine-tuning, then estimate matrix sensitivity through a back-propagation based matrix ranking algorithm, and finally, we perform a linear search for a rank approximation which minimises a parameterised cost function.

### B. Rank Lowering Through Fine-Tuning

In order to lower the effective rank of the FC matrices of our model, we introduce a rank loss function during the fine-tuning stage of training. We first train our model to an acceptable accuracy. them replace all conv. layers in our network with the equivalent FC matrix that will eventually be mapped onto the crossbar, as shown in figure 1a. We then replace our loss function $L(X, Y)$ with

$$L'(X, Y) = L(X, Y) + \lambda \sum_{l=1}^{L_f} \min\{r : \ \sigma_{l,r} \leq \epsilon_l\} \tag{3}$$

where $\sigma_{l,r}$ describes the $r$ singular values of the matrix $l$ of the model $X$, $\epsilon_l$ describe a normalized effective rank parameter defined as $\epsilon_0 \times \sigma_{l,1}$ where $\epsilon_0$ and $\lambda$ are user provided parameters. This added term is defined as the numeric rank of a matrix [17]. A low numeric rank ensures that a low-rank approximation of the matrix remains accurate.

### C. Matrix Ranking Algorithm

In order to characterize the degree of sensitivity of FC matrices and unrolled Conv kernels to the final output accuracy, we use a technique adapted from [18], which uses back-propagation to measure local error gradients of each layer, then average over a number of iterations of training. These local error gradients $\delta$ are then used in the loss function which will

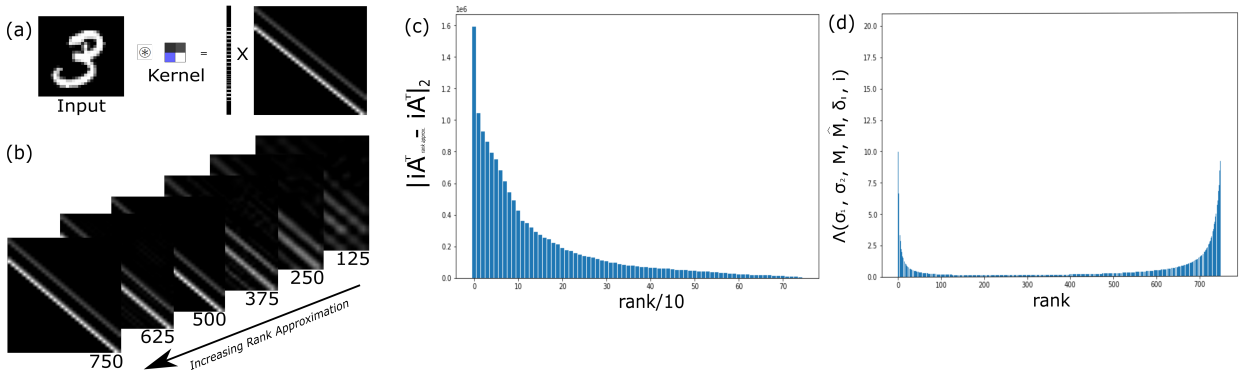


Fig. 2. (a) Illustration of the unrolling of a 28×28 MNIST image convolved with a 2×2 kernel. (b) Illustration of change in unrolled convolution matrix with increasing rank approximations. (c) loss in output accuracy with varying low rank approximations. (d) Low rank Approximator loss function with varying low rank approximations of unrolled LeNet-5 5×5 Conv1 kernel.

**Algorithm 1** Matrix Ranking Algorithm

**Input:** *pretrained model*, *iterations*, *data*
**Output:** *ranked kernels*, *FC*

*Initialize* $\delta_l = 0$
**for** $i$ in iterations **do**
  **for** $l$ in model **do**
    $\epsilon$ = $BackProp(model, data)$
    $\delta_l$ = $\delta_l$ + $\epsilon$
  **end for**
**end for**
$\delta_l$ = $\delta_l / i$

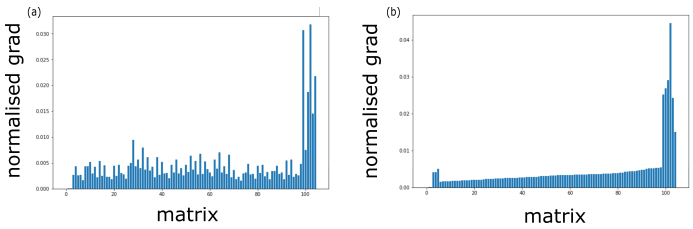


Fig. 3. (a) normalised gradients $\delta_l$ of LeNet-5 FC matrices and unrolled convolution kernels, as they appear in the model (b) ranked normalised gradients.

be used to find the optimal low-rank approximation. This step is performed prior to applying rank regularization. Figure 3 illustrates the ranking of the matrices of a 5 layer CNN, and their respective normalised gradients.

### *D. Low Rank Approximation*

It should be noted that the weight update rule, $\mathbf{G}_{i+1} = \mathbf{G}_i + x^\intercal y$, is sequential, thus the previously applied weights must be considered when reprogramming a crossbar with new weights. One approach to solve this would be to zero the weights prior to reprogramming, this reduces overhead, as you would only need to apply the negative of the already applied column and row vectors and could map any matrix to any crossbar on the fly, however, this approach also doubles the time to map a new matrix. Since our design is primarily concerned

**Algorithm 2** Matrix Low Rank Approximator

**Input:** *ranked matricies*, $\delta$, $\sigma_1$, $\sigma_2$
**Output:** *approximation vectors*

**for** $\mathbf{M}_l$ in *ranked matricies* **do**
  P,D,Q = SVD($\mathbf{M}_l$)
  i = 1
  $\hat{\mathbf{M}}_l$ = $d_i p_{:i} q_{i:}$
  $\lambda_{prev}$ = $\Lambda(\sigma_1, \sigma_2, \mathbf{M}, \hat{\mathbf{M}}, \delta_l, i)$
  **do**
    i += 1
    $\hat{\mathbf{M}}_l$ += $d_i p_{:i} q_{i:}$
    $\lambda_{cur}$ = $\Lambda(\sigma_1, \sigma_2, \mathbf{M}, \hat{\mathbf{M}}, \delta_l, i)$
  **while** $\lambda_{prev} > \lambda_{cur}$ and $i < P.shape[1]$
  $approx.for M_l$ = $\sum^i d_i p_{:i} q_{i:}$
**end for**

with reducing programming delay, we propose computing the SVD of the difference matrix $\mathbf{G}_{i+1} = \mathbf{M}_{i+1} - \mathbf{M}_i$ with $\mathbf{M}_0 = \mathbf{0}$, and applying this during weight update. We also propose the following algorithm to determine the rank of the approximation matrix $\hat{\mathbf{M}}$, the algorithm uses the sensitivity of the matrix obtained from the matrix rank algorithm to arrive at an approximation with high accuracy and low latency.

The Matrix Low Rank Approximator aims to minimise an approximation cost function

$$\Lambda(\sigma_1, \sigma_2, \mathbf{M}, \hat{\mathbf{M}}, \delta_l, i) = \sigma_1 \frac{i}{\delta_l ||\mathbf{M} - \hat{\mathbf{M}}||_F} + \sigma_2 \frac{\delta_l ||\mathbf{M} - \hat{\mathbf{M}}||_F}{i} \tag{4}$$

Loss of accuracy obtained from the $i$th rank approximation represented by the product of the Frobenius norm of $\mathbf{M} - \hat{\mathbf{M}}$, where $\mathbf{M}$ is the initial matrix and $\hat{\mathbf{M}}$ is the $i$ rank approximation of $\mathbf{M}$ and the layer gradient $\delta_l$ obtained from the Matrix Rank algorithm, with the rank of the approximation and two weighting constants $\sigma_1$ and $\sigma_2$, which allow the user to adjust the relative importance of accuracy and delay, in order to obtain an optimal rank. This is done by iteratively increasing the rank until the global minima is found.

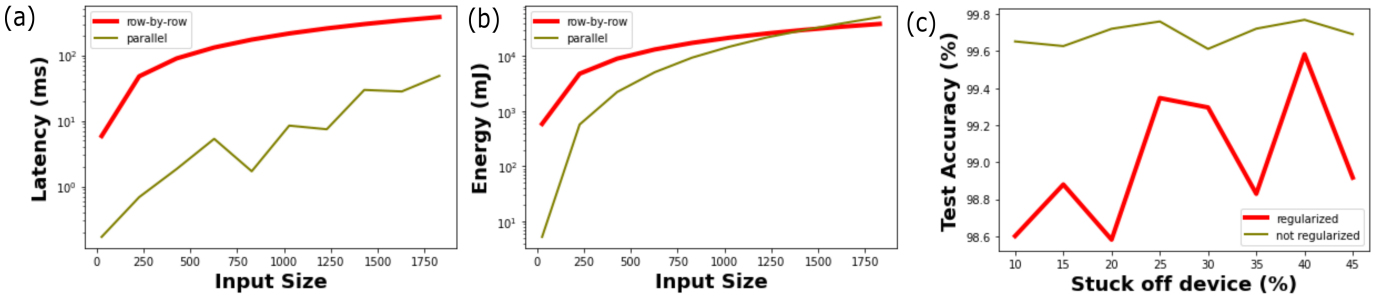


Fig. 4. (a) Programming latency of $5 \times 5$ kernel convoluted with varying input sizes using fully parallel write and sequential write. (b) Energy consumption with varying input sizes. (c) Test accuracy with varying percentages of stuck-off faults, with and without rank regularization.

TABLE I
SVD BASED PARALLEL WRITE PERFORMANCE

| Architecture | LRA Mode | Accuracy (%) | Latency (ms) |
|---|---|---|---|
| LenNet-5 (MNIST) | None | 99.75 | 75 |
| | HA | 98.55 | 50 |
| | LL | 97.83 | 35 |
| VGG-16 (CIFAR-10) | None | 93.51 | 124 |
| | HA | 91.30 | 97 |
| | LL | 88.62 | 52 |

## IV. RESULTS AND DISCUSSION

In this section, we evaluate the inference accuracy, Energy consumption, programming delay and accuracy scaling with stuck-off faults of our SVD based parallel write scheme on a LeNet-5 CNN architecture trained and evaluated on the MNIST dataset. We also evaluate inference accuracy and average kernel write time on the VGG-16 architecture trained and evaluated with the CIFAR-10 dataset. All models are designed and trained using the PyTorch API. All inference accuracy simulations were performed using the MemTorch simulation framework [19] using the VTEAM device model [20] in a 0-Transistor 1-Resistor (0T1R) crossbar configuration. After initial training, all Conv. layers are replaced by equivalent FC layers, then the Matrix Rank algorithm is run to generate the vector of gradients for each matrix used in the model. We then perform fine-tuning with the rank regularization parameters set to $\sigma_0 = 0.02$, $\lambda = 0.005$. We then run the Low Rank Approximator (LRA) algorithm with two modes, a high accuracy mode (HA) and a low latency mode (LL) with LRA coefficients $\sigma_1 = 1, \sigma_2 = 1.7$ and $\sigma_1 = 1.7, \sigma_2 = 1$ respectively. We then compared the inference accuracy and average time to program between architectures and LRA modes and also compare with standard row-by-row crossbar programming.

Finally, we also measured the programming latency and write cycle energy consumption needed to program a $5\times5$ kernel convolution with varying input sizes between a row-by-row write scheme and our parallel write scheme using the LL LRA mode. Simulations for programming latency and energy consumption were adapted from equations outlined by Gao *et al.* [11].

Latency results demonstrate a linear relationship between latency and input size for both parallel and row-by-row writes. While parallel write latency should roughly remain constant with varying crossbar sizes, the need to take many outer product terms causes its latency to scale linearly as well. However, we still see significant decrease in latency with parallel write due to the fact that low rank approximations in LL mode with rank regularization have fewer terms, as demonstrated in fig. 4. Energy consumption with row-by-row writes demonstrates a linear relationship with input sizes, while parallel write demonstrates quadratic scaling. This is to be expected as parallel write energy scales linearly with input size [11], which when coupled with low-rank approximation leads to quadratic scaling. We do, however, see better energy consumption for smaller input sizes, as demonstrated in fig. 4b. Non-ideal behaviour can be attributed to many factors, including imperfect fabrication processes, limited precision in control circuitry and heavy utilisation. Stuck-at-fault [21] are one such fault which is primarily caused by heavy device utilisation. They occur when device conductance states are fixed to a high (stuck-on) or low (stuck-off) state. We measured the effect that stuck-off faults would have on test accuracy with and without applying rank regularization, as an increase in these faults may result from the increased device utilisation incurred from applying constant voltages while writing in parallel. We observed a variable increase in accuracy with higher percentages of stuck-off cells, as demonstrated in figure 4c. This is due to the sparse nature of unrolled convolutions, meaning that more stuck-off cells actually corrects the loss of sparsity obtained from taking a low-rank approximation.

## V. CONCLUSION

In this paper, we proposed an SVD based parallel writing scheme to decrease the programming latency of memristor crossbar tiles. We also proposed an algorithm to find the optimal low rank approximation of model matrices, which minimises programming delay while maximising inference accuracy. Our methods demonstrate a 90% reduction in programming latency needed to program standard CNN architectures, while minimally affecting inference accuracy, decreasing energy consumption for smaller input sizes and increasing resistance to stuck-off faults.

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